CLAIMS:

What is claimed is:

1. A bus design, comprising:

a clock driver;

a clock receiver coupled to the clock driver by two clock bus lines carrying complementary clock pulses;

a plurality of drivers;

a plurality of receivers each coupled to a respective one of the plurality of drivers by bus lines, said receivers detecting signals on respective bus lines with respect to a reference voltage derived from a combination of the complementary clock pulses.

2. The bus as recited in claim 1, wherein said reference voltage is derived from a resistive connection between said complementary clock pulses.

3. The bus as recited in claim 2, wherein the resistors in the resistive connection have an approximately equivalent resistance.

4. The bus as recited in claim 3, wherein the resistance is approximately equivalent to the resistance of the bus lines.

5. The bus as recited in claim 2, further comprising:

a first filter capacitor connecting said reference voltage signal to ground.

6. The bus as recited in claim 5, further comprising:

a second filter capacitor connecting said reference voltage to a supply voltage source.

7. The bus as recited in claim 6, wherein the first and second filter capacitors have an approximately equivalent capacitance.

8. The bus as recited in claim 7, wherein the capacitance is within a range of approximately 100 pico-farads and approximately 200 pico-farads.

9. The bus as recited in claim 1, further comprising:

a plurality of outputs from the data receivers coupled to a deskew/retiming logic component.

10. A data processing system, comprising:

a plurality of components; and

a bus coupling at least two of the plurality of components; wherein the bus comprises:

a clock driver;

a clock receiver coupled to the clock driver by two clock bus lines carrying complementary clock pulses;

a plurality of drivers;

a plurality of receivers each coupled to a respective one of the plurality of drivers by bus lines, said receivers detecting signals on respective bus lines with respect to a reference voltage derived from a combination of the complementary clock pulses.

11. The data processing system as recited in claim 10, wherein said reference voltage is derived from a resistive connection between said complementary clock pulses.

12. The data processing system as recited in claim 11, wherein the resistors in the resistive connection have an approximately equivalent resistance.

13. The data processing system as recited in claim 12, wherein the resistance is approximately fifty ohms.

14. The data processing system as recited in claim 11, further comprising:

a first filter capacitor connecting said reference voltage signal to ground.

15. The data processing system as recited in claim 14, further comprising:

a second filter capacitor connecting said reference voltage to a supply voltage source.

16. The data processing system as recited in claim 15, wherein the first and second filter capacitors have an approximately equivalent capacitance.

17. The data processing system as recited in claim 16, wherein the capacitance is within a range of approximately 100 pico-farads and approximately 200 pico-farads.

18. The data processing system as recited in claim 11, further comprising:

a plurality of outputs from the data receivers coupled to a deskew/retiming logic component.